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Patentanmeldung Nr. Patent application No. Demande de brevet n°

99250347.4

PRIORITY DOCUMENT

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Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
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Blatt 2 der Bescheinigung
Sheet 2 of the certificate
Page 2 de l'attestation

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Method for power level control of a display device and apparatus for carrying out the method

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Method for power level control of a display device and apparatus for carrying out the method

The invention relates to a method for power level control of a display device and an apparatus for carrying out the method.

More specifically the invention is closely related to a kind of video processing for improving the picture quality of pictures which are displayed on displays like plasma display panels (PDP), and all kind of displays based on the principle of duty cycle modulation (pulse width modulation) of light emission.

Background

For image quality, peak white is of paramount importance. The Peak White Enhancement Factor, PWEF, can be defined as the ratio between the peak white luminance level, to the luminance of a homogeneous white field, usually referred to as the full white level. CRT based displays have PWEFs of up to 5, but present Plasma Display Panels, PDPs, have PWEFs of about 2.

A Plasma Display Panel (PDP) utilizes a matrix array of discharge cells, which could only be "ON" or "OFF". Also unlike a CRT or LCD in which grey levels are expressed by analogue control of the light emission, a PDP controls the grey level by modulating the number of light pulses per frame (sustain pulses). This time-modulation will be integrated by the eye over a period corresponding to the eye time response.

More sustain pulses correspond to more peak luminance. More sustain pulses correspond also to a higher power that flows in the PDP. The PDP control can generate more or less sustain pulses as a function of average picture power, i.e., it

switches between modes with different power levels. In this document, the Power Level of a given mode is defined as the number of sustain discharges activated for a region of 100 ire video. The available range of power level modes is approximately equal to the PWEF.

A previous European patent application of the applicant with application number 99101977.9 reports a technique that increases the PWEF of a PDP by increasing the number of available power level modes, in number and in range, and by introducing an hysteresis circuit in the luminance level selection control.

PDPs have a large surface. A PWEF of 5, although pleasant to the image quality, has the disadvantage that it may concentrate, under certain circumstances, for a long time, the power dissipation on a small surface of the panel. If this situation is prolonged for a large time, which may occur in case of still video, local overheating of the panel may assume unacceptable values. The present invention concerns a protection circuit to be used in combination with any peak white enhancement circuit, not only for PDPs, having a large PWEF factor.

This protection circuit is based on the circuit described in another European patent application of the applicant with application number 99112906.5.

First generation of PDPs were characterised by having a peak white to maximum average luminance ratio of about 2. This is far worse than what is achieved in old CRT technology, where factors up to 5 are normal.

New developments allow achieving factors up to 5, also for PDP based displays. However, high values of the PWEF, are prone to local overheating of display, in case of still

video. This is a seriously problem, that would limit, without a protection circuit, the achievable PWEF value.

This invention describes a thermal protection circuit for displays having a large PWEF, which comprise some or all of the following circuits:

1. Local power measurement circuit.

2. Local temperature estimator circuit.

3. Evaluator of the maximum of the local temperature function.

4. Selector of the maximum allowed power level, as a function of the estimated maximum local temperature value. This function should include hysteresis, in order to prevent the occurrence of perceivable luminance oscillations.

5. Limiter of the current power level value, to the selected maximum allowed power level. This limiter actually performs the protection function.

One main idea behind this invention is to try to build a model that describes local overheating of a panel as a function of displayed video, and to use that information to control the operation of the peak white enhancement loop.

Example

The principles behind this invention are now explained by means of an example. It should be here strongly noted that values in an actual implementation may differ from those here shown, in particular the number and weight of the used subfields and the number of actual sustain pulses.

The example explained here, is based on an example shown in European Patent Application 99101977.9 of the applicant. For the disclosure of the invention it is therefore also referred to the content of this application.

Supposed is a PDP display with PWEF of 5. Video is coded from 0 to 255. Power level control generates a maximum of 5*255 sustain pulses (peak white) and a minimum of 255 pulses (full white), for 100 ire, in the mode with lower power level. PWEF = (5*255)/255 = 1;

A solution was described using 4 different main modes:

Mode 1: 12 sub-fields (2*255 sustain pulses):
1 - 2 - 4 - 8 - 16 - 32 - 32 - 32 - 32 - 32 - 32 - 32

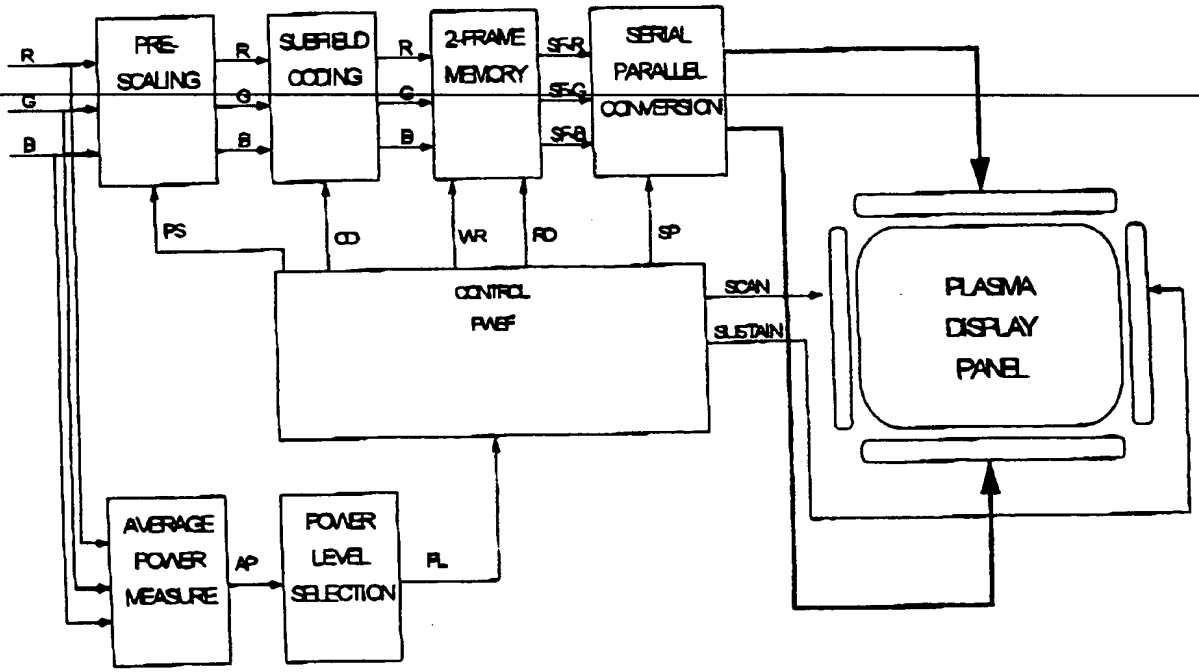
Mode 2: 11 sub-fields (3*255 sustain pulses):
1 - 2 - 4 - 8 - 16 - 32 - 32 - 40 - 40 - 40 - 40

Mode 3: 10 sub-fields (4*255 sustain pulses):
1 - 2 - 4 - 8 - 16 - 32 - 48 - 48 - 48 - 48

Mode 4: 9 sub-fields (5*255 sustain pulses):
1 - 2 - 4 - 8 - 16 - 32 - 64 - 64 - 64

Each of these 4 modes is subdivided in about 16 sub-modes, which use the same number of sub-fields, but which encode 100 ire to a different value (dynamic pre-scaling). A total of 64 sub-modes were listed, corresponding to 64 power levels (number of sustain pulses for 100 ire), increasing gradually from 255 to 1275.

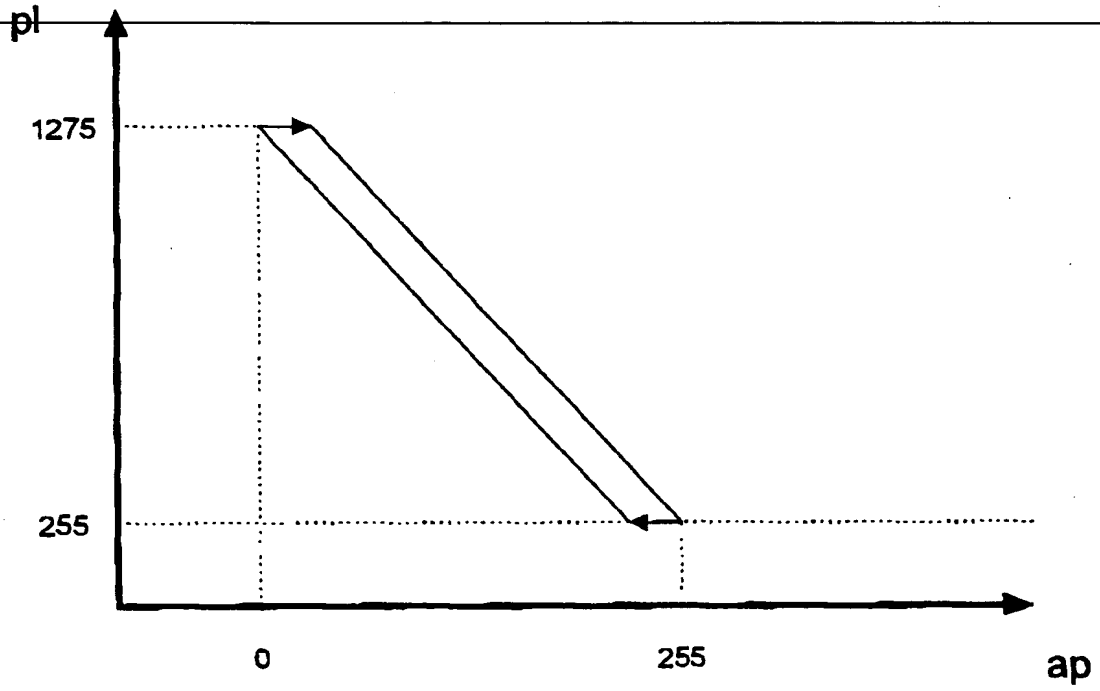
The peak white enhancement circuit without any protection circuit as disclosed in EP 99101977.9 is shown in the next figure.



RGB data is analysed on the average power measure block which gives the computed average power value (AP) to the PWEF control block. The PWEF control block, consults its internal power level mode table, taking in consideration the previous measured value (hysteresis), and directly generates the selected mode control signals for the other processing blocks. It selects the pre-scaling factor (PS) and the sub-field code to be used (CD). It also controls the writing of RGB pixel data in the frame memory (WR), the reading of RGB sub-field data from the second frame memory (RD), and the serial to parallel conversion circuit (SP). Finally it generates the SCAN and SUSTAIN pulses required to drive the PDP driver circuits.

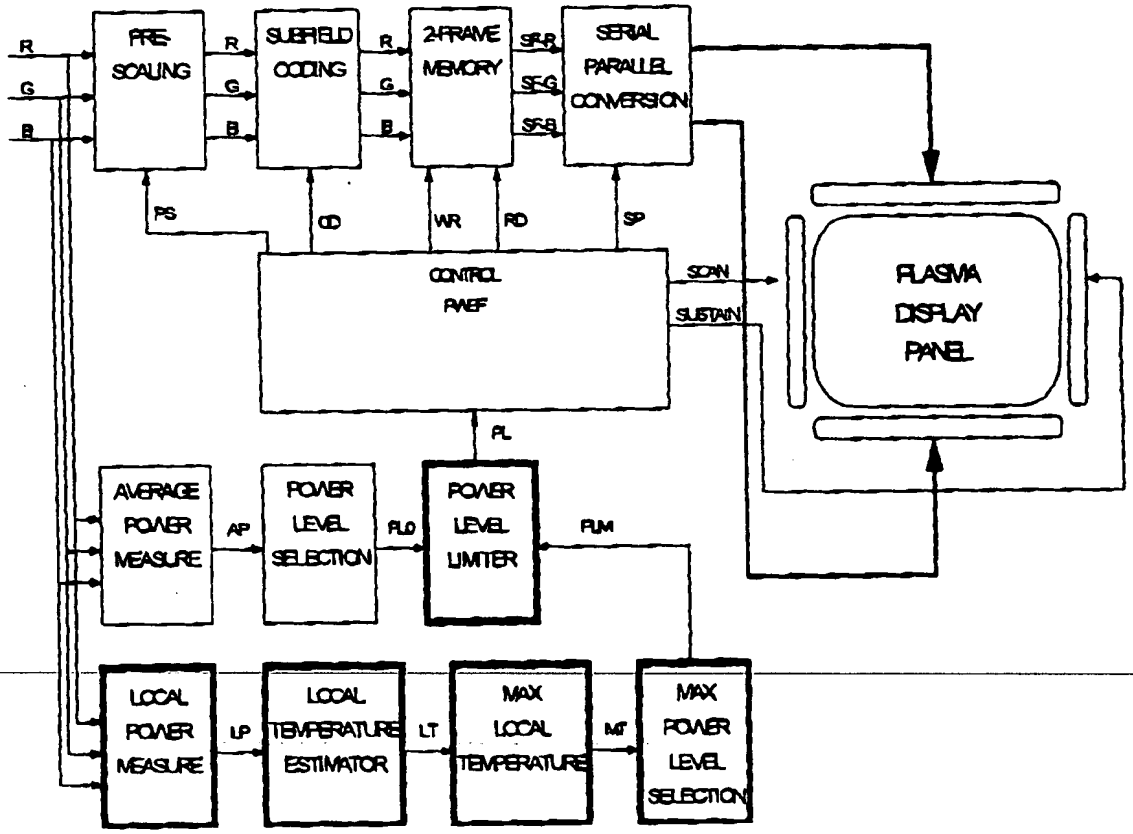
Power level selection

The following figure, also already shown in patent application EP 99101977.9, shows a possibility for the dynamic control of the power level selection (pl) as a function of the measured picture average power (ap):



As it should be expected, when picture power level increases, modes are selected with decreasing power levels. There is an hysteresis loop in the control function. When picture average power is increasing, modes with power levels on the top line are chosen. When picture power is decreasing, modes with power levels on the bottom line are chosen. Points between the two lines can be chosen when the picture average power growth direction is modified.

Peak white enhancement circuit with protection



The figure above depicts a peak white enhancement circuit with a protection circuit, which is the core of this invention. The blocks drawn in bold correspond to the blocks that constitute the protection circuit.

1. Local power measure

One main idea is to divide the total display surface in many cells S_{ij}, and then to integrate (add) input video levels for all pixels, and for the 3 colour components, belonging to a given cell, obtaining value P_{ij}:

$$P_{ij} = \Sigma(k \in S_{ij}) \ (R_k + G_k + B_k)$$

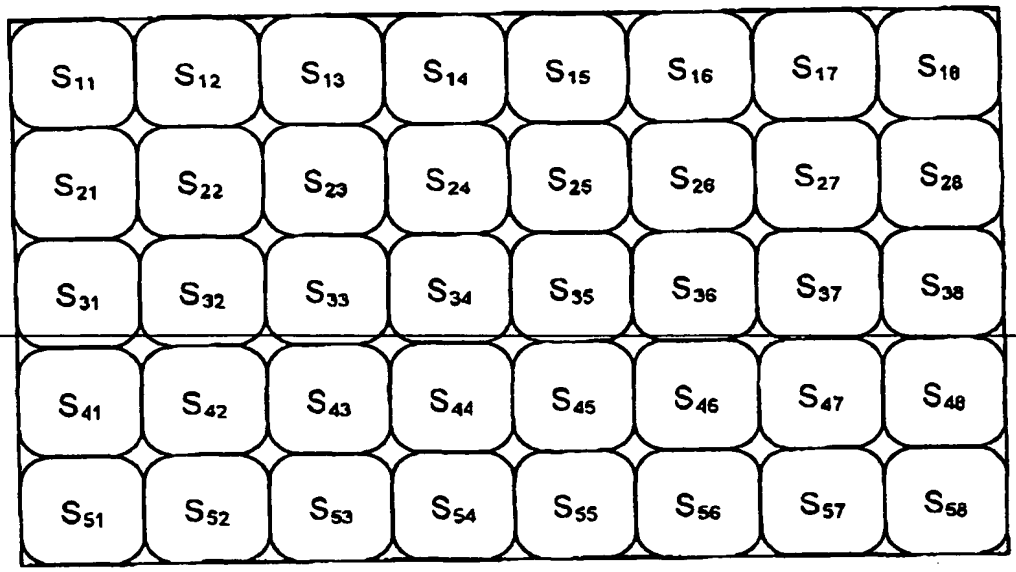
where k denotes all pixels belonging to S_{ij}.

Very bright small spots may be more objectionable than spots, having the same total power, but being somewhat larger. To handle this fact, it is suggested to square or even to cube the RGB pixel components:

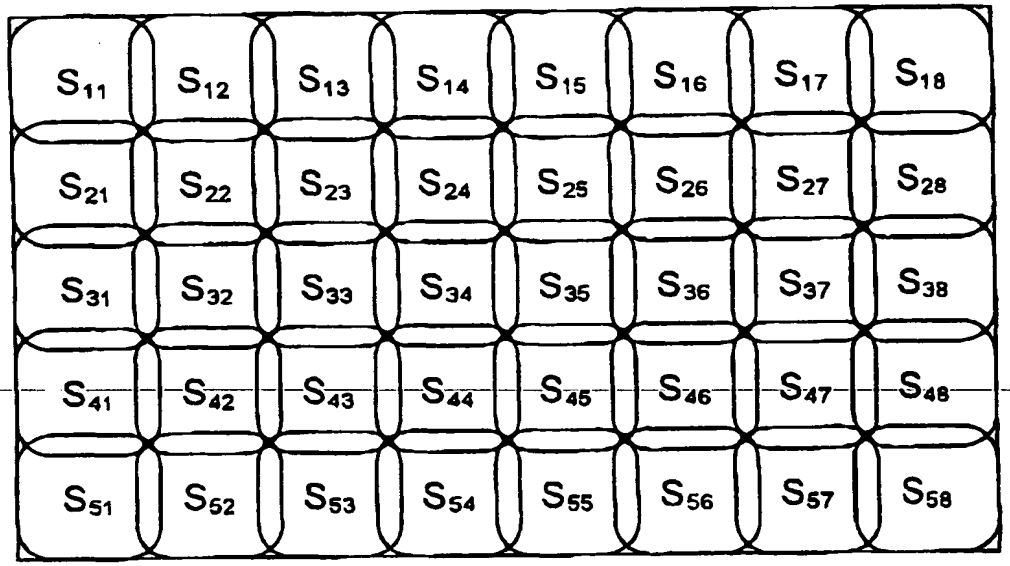
$$P_{ij} = \Sigma(k \in S_{ij}) \ (R_k^2 + G_k^2 + B_k^2)$$

$$P_{ij} = \Sigma(k \in S_{ij}) \ (R_k^3 + G_k^3 + B_k^3)$$

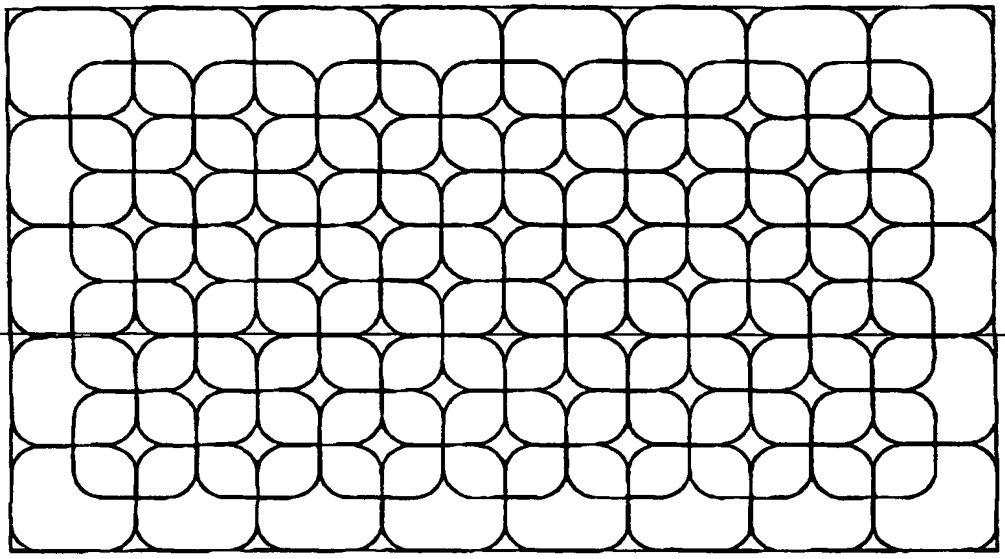
In the figure below, an example is shown of the division of the plasma display surface in cells S_{ij}. For easiness of visualization, cells are presented with rounded edges, but in a practical implementation they will preferably be rectangular. On the shown example there is a total of 40 cells, but in an actual implementation the cell number might even be higher.



The partition of the total display surface in cells S_{ij} can be improved, if overlapping of cells is allowed, as shown in the figure below:



Another possibility is to use diagonal overlapping:



Without overlapping of cells, if a bright spot occurs, for instance exactly at the border of 2 cells, it might not be detected. With substantial overlapping of cells, there will always be a cell that comprises any bright spot, regardless of the bright spot position.

2. Local temperature estimator

If the power being dissipated has been evaluated, the next step is to build a model that associates to every cell a local temperature value. It should be here pointed out that many models are possible, some very simple, some quite complex, and that a compromise in complexity will have to be found. Here, some of the possible approaches are mentioned, keeping in mind that even the simplest approximation is better than having no protection at all.

The temperature of a given cell is, in a first approximation, equal to the previous temperature estimation, plus the power being dissipated P(i,j), minus a dissipation term corresponding to the heat being given to the environment per frame time:

$$T(i,j)_t = T(i,j)_{t-1} + a\ P(i,j)_t - D$$

This model can be improved if we make the assumption that heat dissipation is proportional to the actual temperature:

$$T(i,j)_t = T(i,j)_{t-1} + a\ P(i,j)_t - b\ T(i,j)_{t-1}$$

Furthermore, thermal dispersion to the near-by cells can also be considered:

$$\begin{aligned} T(i,j)_t = {} & T(i,j)_{t-1} + a\ P(i,j)_t - b\ T(i,j)_{t-1} - \\ & c\ [\ T(i-1,j)_{t-1} - T(i,j)_{t-1}\ ] - \\ & c\ [\ T(i+1,j)_{t-1} - T(i,j)_{t-1}\ ] - \\ & c\ [\ T(i,j-1)_{t-1} - T(i,j)_{t-1}\ ] - \\ & c\ [\ T(i,j+1)_{t-1} - T(i,j)_{t-1}\ ] \end{aligned}$$

The newly added terms can be either negative (if the near-by cells are cooler) or positive (if the near-by cells are hotter). Finally, for a last further refinement, diagonal thermal dispersion might also be considered by adding 4 further terms, but the complexity of the shown model should be enough for all practical purposes.

The above model also deals with the border effect. Cells at the border, or at the corners will have less dissipation possibilities, due to the fact that they have less near-by cells. They may overheat quicker, for the same power being dissipated, but this should be correctly detected by the last here presented model.

3. Maximum local temperature

In principle to find the maximum local temperature MT, it is only required to evaluate, in the current example, the 40 P_{ij} values (40 = 5 rows * 8 columns) and the corresponding

40 T_{ij} values, and then finding the maximum. This requires quite a number of operations per frame, with a large number of video integrators working in parallel.

Thermal heating is however a very slow process, and so the following approximation might be used:

1. For every frame the dissipation on a single cell is calculated, i.e., power dissipation in every cell is evaluated once for every group of 40 frames (in this example).

2. For the selected cell the local temperature is computed using the following expression:

$$T(i,j)_t = T(i,j)_{t-40} + a\,P(i,j)_t - b\,T(i,j)_{t-40} - c\,[\,T(i-1,j)_{t-40} - T(i,j)_{t-40}\,] - c\,[\,T(i+1,j)_{t-40} - T(i,j)_{t-40}\,] - c\,[\,T(i,j-1)_{t-40} - T(i,j)_{t-40}\,] - c\,[\,T(i,j+1)_{t-40} - T(i,j)_{t-40}\,]$$

3. Update the MT value (maximum temperature). In order to do this it is required to know whether cell number (i,j) being evaluated, corresponds to the cell (i,j)max where previous MT value (Mt_{t-1}) was found.

If cell number is the same ((i,j) = (i,j)max):

$MT_t = T_{ij}$

If cell number is not the same ((i,j) ≠ (i,j)max):

if ($T_{ij} > MT_{t-1}$)

then $MT_t = T_{ij}$

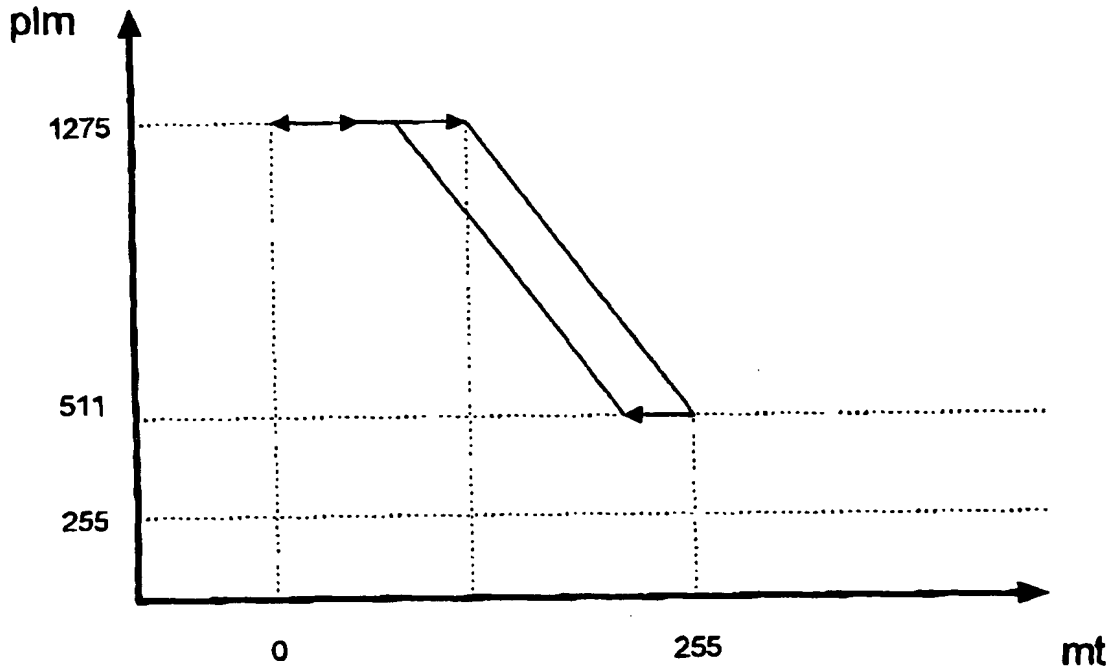
and (i,j)max = (i,j)

else

$MT_t = MT_{t-1}$

The above mentioned approximation reduces evaluation complexity by a factor of 40.

4. Maximum power level selection



This figure depicts the function of the maximum power selection circuit. It shows the maximum allowed power level (plm) as a function of the estimated maximum panel local temperature (mt).

For low limits of maximum local temperature, no reductions in peak white level are required. For higher levels, maximum peak white level is gradually reduced. At the limit, in the above example, PWEF has been reduced from the original value of 5 to approximately 2 (full white corresponds to a power level of 255).

Some hysteresis is built-in, in order to avoid small amplitude oscillations, mostly originating in errors of measurement, or in the displayed video noise.

A final remark: the temperature model is a model that reacts slowly to modifications in dissipated power. This is correct, because panel temperature also reacts slowly to power being dissipated. Due to this slow reaction of the estimated panel temperature, the protection circuit will also react slowly, which has the additional advantage that its operation will be not be perceived by the human viewer.

5. Power level limiter

This circuit is a simple limiter that actuates only when dangerous local overheating has been detected. It interferes in no way in the operation of the peak white enhancement circuit. It only limits the power range available to the peak white enhancement control circuit.

This is a protection circuit, which means that, for most video, it will have no effect, and only in case of a static bright spot, the peak white enhancement factor will be attenuated.
It can also be used for CRT based displays, where local overheating may cause local doming problems. Local doming, is a colour distortion of the picture, due to the local deformation of the CRT's mask, which is induced by local overheating of the tube colour mask.

It is also possible to have dynamic peak white control without having a protection circuit. Picture quality will however not be the same, because the dynamic peak white control will use a restricted range for the PWEF, in order to avoid unacceptable local thermal overheating.

Claims

1. Method for power level control in a display device having a plurality of luminous elements corresponding to the pixels of a picture, wherein a power level mode selection process is used for increasing the peak white ~~enhancement factor of the display, characterised in that~~ a picture is divided in a number of cells, wherein in each cell the video levels or values derived from the video levels of the colour components of the pixels are summed up in order to determine the local power values for the picture, wherein a local temperature estimation is performed based on said local power values, wherein a step of determining the maximum local temperature in the display is performed and wherein the maximum allowed power level limit of the display is adjusted based on the maximum local temperature value and wherein the power level limit influences the power level mode selection process.

2. Method according to claim 1, wherein for local temperature estimation of a cell the power dissipation not only of the local cell but also of a number of neighbouring cells is taken into account.

3. Method according to claim 1 or 2, wherein maximum local temperature determination for the display is performed once in a number of video frames.

4. Method according to claim 3, wherein the steps of local power value determination and local temperature estimation are performed for one or more selected cells within a frame period only.

5. Method according to claim 3 or 4, wherein a picture is divided in 40 cells and maximum local temperature determination is performed once within 40 frame periods.

6. Method according to one of claims 1 to 5, wherein the switching between maximum allowed power level limits corresponding to the determined maximum local temperature is controlled with an hysteresis-like switching behaviour.

7. Apparatus for carrying out the method according to one of the previous claims, characterised in that, it includes a power level determination and selection circuit, a local power measuring unit, a local temperature estimator, a maximum local temperature determination unit, a maximum power level limit selector and a power level limiter for correcting a selected power level mode for the display if the power level of the selected mode exceeds the selected maximum power level limit.

8. Apparatus according to claim 7, wherein it is integrated in a display device, in particular plasma display device.

Abstract

Method for power level control of a display device and apparatus for carrying out the method

Plasma Display Panels (PDP) are becoming more and more interesting for TV technology. One important criterion for picture quality is the Peak White Enhancement Factor PWEF. In a previous patent application a method for power level control in a display with which the PWEF can be increased has been proposed. With an increased PWEF the problem of local overheating of plasma cells may occur.
This invention proposes a protection circuit, which deals with this problem. For protecting the plasma display against local overheating, there is provided a method, which performs the steps of local power value determination, local temperature estimation, maximum local temperature determination and maximum power level limit determination. The power level limit influences the power level control process in the display device so that local overheating is avoided and the highest possible PWEF can be used. The invention also concerns a corresponding apparatus for carrying out the proposed method.

Fig. 3